

WHAT IS CLAIMED IS:

1 1. A power monitor circuit capable of notifying processing
2 circuits operating from a first power supply having a VDD output
3 voltage when a second power supply having a VDDIO output voltage
4 is powered up, wherein VDDIO is greater than VDD, said power
5 monitor circuit comprising:

6 a voltage divider circuit coupled between said second
7 power supply and ground and having an output node that rises to a
8 high voltage when said second power supply is powered up; and

9 an odd number of serially connected inverters operating
10 from said first power supply, wherein an input of a first of said
11 serially connected inverters is connected to said voltage divider
12 circuit output node and an output of a last of said serially
13 connected inverters produces a status signal that is low when
14 said voltage divider circuit output node is high and is high when
15 said voltage divider circuit output node is low, and wherein said
16 status signal is an input signal to said voltage divider circuit
17 operable to minimize DC current consumption in said voltage
18 divider circuit when said second power supply is powered up while
19 maintaining a value of said status signal.

1 2. The power monitor circuit as set forth in Claim 1
2 wherein said serially connected inverters comprise CMOS
3 inverters.

1 3. The power monitor circuit as set forth in Claim 1
2 wherein said voltage divider circuit comprises: 1) a first N-
3 channel transistor having a gate and a drain coupled to said
VDDIO output voltage and a source coupled to said voltage divider
circuit output node; 2) a second N-channel transistor having a
gate coupled to said VDD output voltage and a drain coupled to
said voltage divider circuit output node; and 3) a third N-
channel transistor having a gate coupled to said status signal, a
drain coupled to a source of said second N-channel transistor,
and a source coupled to ground.

1 4. The power monitor circuit as set forth in Claim 3
2 further comprising a capacitor coupled between said voltage
3 divider circuit output node and ground.

1 5. The power monitor circuit as set forth in Claim 4
2 further comprising a fourth N-channel transistor having a gate
3 coupled to said VDD output voltage, a drain coupled to said VDDIO
4 output voltage, and a source coupled to said voltage divider
5 circuit output node.

1 6. The power monitor circuit as set forth in Claim 1
2 wherein said odd number of serially connected inverters comprises
3 one inverter.

1 7. The power monitor circuit as set forth in Claim 6
2 wherein said odd number of serially connected inverters comprises
3 one CMOS inverter.

1 8. The power monitor circuit as set forth in Claim 1
2 wherein said odd number of serially connected inverters comprises
3 three inverters.

1 9. The power monitor circuit as set forth in Claim 8
2 wherein said odd number of serially connected inverters comprises
3 three CMOS inverters.

1 10. The power monitor circuit as set forth in Claim 1
2 wherein said odd number of serially connected inverters comprises
3 five inverters.

1 11. The power monitor circuit as set forth in Claim 10
2 wherein said odd number of serially connected inverters comprises
3 five CMOS inverters.

1 12. An integrated circuit comprising:

2 core processing circuitry operating from a first power
3 supply having a VDD output voltage;

4 output stage circuitry operating from a second power
5 supply having a VDDIO output voltage, wherein VDDIO is greater
6 than VDD; and

7 a power monitor circuit capable of notifying said core
8 processing circuitry when said second power supply having said
9 VDDIO output voltage is powered up, said power monitor circuit
10 comprising:

11 a voltage divider circuit coupled between said
12 second power supply and ground and having an output node
13 that rises to a high voltage when said second power supply
14 is powered up; and

15 an odd number of serially connected inverters
16 operating from said first power supply, wherein an input of
17 a first of said serially connected inverters is connected
18 to said voltage divider circuit output node and an output
19 of a last of said serially connected inverters produces a
20 status signal that is low when said voltage divider circuit
21 output node is high and is high when said voltage divider
22 circuit output node is low, and wherein said status signal
23 is an input signal to said voltage divider circuit operable
24 to minimize DC current consumption in said voltage divider

25 circuit when said second power supply is powered up while
26 maintaining a value of said status signal.

1 13. The integrated circuit as set forth in Claim 12 wherein
2 said serially connected inverters comprise CMOS inverters.

1 14. The integrated circuit as set forth in Claim 12 wherein
2 said voltage divider circuit comprises: 1) a first N-channel
3 transistor having a gate and a drain coupled to said VDDIO output
4 voltage and a source coupled to said voltage divider circuit
5 output node; 2) a second N-channel transistor having a gate
6 coupled to said VDD output voltage and a drain coupled to said
7 voltage divider circuit output node; and 3) a third N-channel
8 transistor having a gate coupled to said status signal, a drain
9 coupled to a source of said second N-channel transistor, and a
10 source coupled to ground.

1 15. The integrated circuit as set forth in Claim 14 further
2 comprising a capacitor coupled between said voltage divider
3 circuit output node and ground.

1 16. The integrated circuit as set forth in Claim 15 further
2 comprising a fourth N-channel transistor having a gate coupled to
3 said VDD output voltage, a drain coupled to said VDDIO output
4 voltage, and a source coupled to said voltage divider circuit
5 output node.

1 17. The integrated circuit as set forth in Claim 12 wherein
2 said odd number of serially connected inverters comprises one
3 inverter.

1 18. The integrated circuit as set forth in Claim 17 wherein
2 said odd number of serially connected inverters comprises one
3 CMOS inverter.

1 19. The integrated circuit as set forth in Claim 12 wherein
2 said odd number of serially connected inverters comprises three
3 inverters.

1 20. The integrated circuit as set forth in Claim 19 wherein
2 said odd number of serially connected inverters comprises three
3 CMOS inverters.

1 21. The integrated circuit as set forth in Claim 20 wherein
2 said odd number of serially connected inverters comprises five
3 inverters.

1 22. The integrated circuit as set forth in Claim 21 wherein
2 said odd number of serially connected inverters comprises five
3 CMOS inverters.